



Terms used **fifo length**

Found **2,474** of **164,603**

Sort results
by

relevance



[Save results to a Binder](#)

Try an [Advanced Search](#)

Try this search in [The ACM Guide](#)

Display
results

expanded form



[Search Tips](#)

☐ Open results in a new window

Results 1 - 20 of 200

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Benchmarking a vector-processor prototype based on multithreaded streaming/FIFO vector \(MSFV\) architecture](#)

Tetsuo Hironaka, Takashi Hashimoto, Keizo Okazaki, Kazuaki Murakami, Shinji Tomita
August 1992 **Proceedings of the 6th international conference on Supercomputing**

Full text available: pdf(1.16 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents the benchmark results on a vector-processor prototype based on the MSFV (multithreaded streaming/FIFO vector) architecture. The MSFV architecture is single-chip oriented, and thus its main object is to save the off-chip memory bandwidth by exploiting the register bandwidth instead. The register bandwidth is exploited by the synergism of FIFO register, chaining, streaming, and multithreading. This paper tries to identify ...

2 [Functional test for shifting-type FIFOs](#)

A. J. van de Goor, I. Schanstra, Y. Zorian

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available: pdf(622.82 KB)

Additional Information: [full citation](#), [abstract](#)



[Publisher Site](#)

FIFO memories impose special test problems because of their built-in addressing restrictions and access limitations. With the increasing use of FIFOs, as a stand-alone chip or as embedded macros in ASICs, generic algorithms are needed to test FIFOs. This paper addresses the problem of testing the widely available shifting-type FIFOs; it introduces specific fault models and a set of generic tests which have a test length of $O(n)$ and can be used for the stand-alone chip as well as for the embedded ...

Keywords: ASIC embedded macro, FIFO memories, fault diagnosis, fault models, functional test, generic tests, integrated circuit testing, integrated memory circuits, logic testing, shifting-type FIFOs, stand-alone chip

3 [Tuning RED for Web traffic](#)

Mikkel Christiansen, Kevin Jeffay, David Ott, F. Donelson Smith

August 2000 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, Technologies, Architectures, and Protocols for Computer Communication**, Volume 30 Issue 4



USPTO

[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)Search: ☒ The ACM Digital Library ☐ The Guide[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

Terms used

fifo length comparator counter pointer multiplexer multiplexor

Found 25 of 164,603

Sort results
by[Save results to a Binder](#)Try an [Advanced Search](#)Display
results[Search Tips](#)Try this search in [The ACM Guide](#)☐ Open results in a new
window

Results 1 - 20 of 25

Result page: [1](#) [2](#) [next](#)Relevance scale ☐ ☐ ☐ ☐ ☐**1 Performance optimization of wireless local area networks through VLSI data compression**

Bongjin Jung, Wayne P. Burleson

January 1998 **Wireless Networks**, Volume 4 Issue 1Full text available: [pdf\(664.69 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In contrast to wireline communication, the physical bandwidth of RF wireless communication systems is relatively limited and is unlikely to grow significantly in the future. Hence it is advantageous to increase the effective bandwidth of communication channels at the expense of complex processing at both the sending and receiving entities. In this paper we present a real-time, low-area, and low-power VLSI lossless data compressor based on the first Lempel-Ziv algorithm (Ziv and Lempel, 1977 ...

2 Dynamic vectorization: a mechanism for exploiting far-flung ILP in ordinary programs

Sriram Vajapeyam, P. J. Joseph, Tulika Mitra

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2Full text available: [pdf\(103.41 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)[Publisher Site](#)

Several ILP limit studies indicate the presence of considerable ILP across dynamically far-apart instructions in program execution. This paper proposes a hardware mechanism, *dynamic vectorization (DV)*, as a tool for quickly building up a large logical instruction window. Dynamic vectorization converts repetitive dynamic instruction sequences into vector form, enabling the processing of instructions from beyond the corresponding program loop to be overlapped with the loop. This enables vec ...

3 A pipelined, multiprocessor architecture for a connectionless server for broadband ISDN

Daniel S. Omundsen, A. Roger Kaye, Samy A. Mahmoud

April 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 2Full text available: [pdf\(1.21 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)